Amendments to the Claims

1. (Currently Amended) A BIST (built-in self test) circuit comprising:

a controller for controlling a self-testing operation of a memory chip embedded in an integrated circuit;

an address generator for generating pseudo-random address patterns comprising address bits, under control of the controller;

a data generator for producing test data ~~associated with~~based on data backgrounds ~~of the~~associated with the address bits and a non-address bit, under the control of the controller; and

a comparator for comparing the test data with memory data output from the memory chip to ~~detect, a defect, if any,~~test ~~of~~ the memory chip.

2. (Currently Amended) The circuit of claim 1, wherein the controller ~~operates using an algorithm that counts the data backgrounds of the address bits in~~implements a single-order test method.

3. (Original) The circuit of claim 1, wherein the address generator comprises:

a plurality of linear feedback shift registers (LFSRs) serially connected to each other for producing the pseudo-random address patterns, the pseudo-random address patterns being single-order pseudo-random address patterns; and

a register controller for controlling the plurality of LFSRs.

4. (Currently Amended) The circuit of claim 3, wherein the [[a]] plurality of LFSRs comprise a counter for counting the address bits to produce the pseudo-random address patterns.

5. (Currently Amended) The circuit of claim 1, wherein the data generator comprises:

a first multiplexer for receiving input values of the address bits and ~~a ground voltage~~the non-address bit, ~~as input values~~ and ~~selecting~~ outputting one of the input values in response to a first control signal from the BIST controller; and

a second multiplexer for ~~producing the test data from the~~selecting the output value of the first multiplexer or its compliment, in response to a second control signal from the controller.

6. (Canceled)

7. (Original) The circuit of claim 1, wherein the address generator comprises:

a first linear feedback shift register for producing a first group of the pseudo-random address patterns by counting the address bits;

a second linear feedback shift register, serially connected to the first linear feedback shift register, for producing a second group of the pseudo-random address patterns by counting the address bits; and

a register controller for controlling the first and second linear feedback shift registers such that the first linear feedback shift register counts lower bits of the address

bits and the second linear feedback shift register counts upper bits of the address bits or the first linear feedback shift register counts upper bits of the address bits and the second linear feedback shift register counts lower bits of the address bits.

8. (Currently Amended) The circuit of claim 7, wherein the pseudo-random ~~random~~ address patterns comprises ~~a single random~~single-order pseudo-random address patterns.

9. (Original) The circuit of claim 7, wherein the second linear feedback shift register produces the second group of the pseudo random address patterns whenever the first linear feedback shift register produces all the first group of the pseudo random address patterns.

10. (Currently Amended) The circuit of claim 1, wherein the data backgrounds ~~of the address bits comprises~~comprise data combinations ~~that~~ of two random memory cells having mutually different addresses ~~have~~.

11. (Currently Amended) A method for performing self-testing operation on a memory chip embedded in an integrated circuit, comprising the steps of:

counting address bits to produce a test address[[es]] ~~of~~ from pseudo-random address patterns comprising address bits;

producing test data ~~according to~~based on ~~the test address and~~ data backgrounds ~~of~~ associated with the address bits and a non-address bit; and

comparing the test data with memory data output from the memory chip to ~~determine whether a defect exists~~ test the memory chip.

12. (Currently Amended) The method of claim 11, wherein the step of counting the address bits comprises the step of counting the data backgrounds ~~of~~ associated with the address bits in a single-order.

13. (Currently Amended) The method of claim ~~12~~11, wherein the step of counting the address bits further comprises the steps of:

counting lower bits of the address bits to produce a first group of the pseudo-random address patterns; and

counting upper bits of the address bits to produce a second group of the pseudo-random address patterns.

14. (Currently Amended) The method of claim 11, wherein the step of producing the test data comprises the steps of:

receiving data values of the address bits and ~~a ground voltage~~the non address bit ~~as input values~~;

selecting one of the ~~input~~ data values in response to a first signal~~, the first signal comprising information about a current data background of the address bits~~; and

~~producing the test data in response to the selected input value and a second signal, the second signal comprising information about a complemented data background of the address bits~~ outputting the selected data value or its complement in response to a second signal.